

FEB 20 2003
U.S. PATENT & TRADEMARK OFFICE

TECHNOLOGY 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 202887US2		SERIAL NO. 09/778,104	
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Yuuichi HIRANO, et al.					
		FILING DATE February 7, 2001		GROUP 2826			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
VAMS	AW	Don Monroe, Jack Hergenrother, The Vertical Replacement Gate (VRG) Process for Scalable General-purpose Complementary Logic, Bell Labs, Lucent Technologies, Murray Hill, NJ					
	AX						
	AY						
	AZ	<input type="checkbox"/> Additional References sheet(s) attached					
Examiner	Victor A. Mandala Jr.			Date Considered 5-14-03			
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							